Taxonomy of Flynn (1966).

To describe these non-von Neumann or parallel architectures, a generally accepted taxonomy is that of Flynn (1966). The classification is based on the notion of two streams of information flow to a processor: instructions and data. These two streams can be either single or multiple, giving four classes of machines:

1. Single instruction single data (SISD)
2. Single instruction multiple data (SIMD)
3. Multiple instruction single data (MISD)
4. Multiple instruction multiple data (MIMD)

Table 5.4 shows the four primary classes and some of the architectures that fit in those classes. Most of these architectures will be briefly discussed.

5.4.2.1 Single Instruction Single Data

The SISD architectures encompass standard serial von Neumann architecture computers. In a sense, the SISD category is the base metric for Flynn's taxonomy.

5.4.2.2 Single Instruction Multiple Data

The SIMD computers are essentially array processors. This type of parallel computer architecture has n-processors, each executing the same instruction, but on different data streams. Often each element in the *array* can only communicate with its nearest neighbour. Computer architectures that are usually classified as SIMD are the *systolic*

TABLE 5.4
Flynn's Classification Scheme for Parallel Computer Architectures

	Single Data Stream	Multiple Data Stream
Single Instruction Stream	von Neumann processors	Systolic processors
	RISC	Wave-front processors
Multiple Instruction Stream	Pipelined architectures	Data flow processors
	VLIW processors	Transputers
		Grid computers
		Multiprocessors

and wave-front array computers. In both types of processor, each processing element executes the same (and only) instruction, but on different data. Hence these architectures are SIMD. SIMD machines are widely used for such *imaging computation* as *matrix arithmetic and convolution*.

5.4.2.3 Multiple Instruction Single Data

The MISD computer architecture lends itself naturally to those computations requiring an input to be subjected to several operations, each receiving the input in its original form. These

applications include classification problems and *digital signal processing*. MISD architectures include *PIPELINED* and very long instruction word architectures (*VLIW*). In pipelined architectures, more than one instruction can be processed simultaneously (one for each level of pipeline). Similarly, VLIW computers tend to be implemented with microinstructions that have very long bit-lengths (and hence more capability). Thus, rather than breaking down macroinstructions into numerous microinstructions, several (nonconflicting) macroinstructions can be combined into several microinstructions.

5.4.2.4 Multiple Instruction Multiple Data

MIMD computers involve large numbers of processors capable of executing more than one instruction on more than one datum at any instant. Except for networks of distributed multiprocessors working on the same problem (grid computing), these are "exotic" architectures. MIMD computers include *data flow computers, grid computers, networks of heterogeneous processors*, and *transputers*.

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